

# Memory Integration Module

## Summary

The memory integration module is responsible for controlling the transfer of the information between the internal C\*CORE local bus and the internal or external asynchronous memory or memory-mapped modules. Up to three asynchronous chip select channel are available, two select (CS0, CS1) for the external memory, one for the external nand-flash.

## Features

- Reduced system complexity — No external glue logic required for typical systems if chip selects are used.
- Three programmable asynchronous active-low chip selects can be independently programmed with various features.
- Control for external boot device — CS0 can be selected as an external 16bit boot device when in master mode.
- Fixed base addresses with 64-Mbyte block sizes
- Support for 8-bit 16-bit and 32-bit devices — The port size can be programmed to be 8, 16 or 32 bits.
- Programmable write protection — Each chip select address range can be designated for read access only.
- Programmable access protection — Each chip select address range can be designated for supervisor access only.
- Write-enable selection — The enable byte pins (EB [3:0]) can be configured as byte enables (assert on both external read and write accesses) or write enables (only assert on external write accesses).
- Bus cycle termination — The chip select logic to terminate the bus cycle.
- Programmable wait states — To interface with various devices, up to seven wait states can be programmed before the access is terminated.
- Programmable extra wait state for write accesses — One wait state can be added to write accesses to allow writing to memories that require additional data setup time.

To obtain more information about the Memory Integration or other C\*Core<sup>TM</sup> products, please contact the C\*Core Technology Co., Ltd. by phone: 0512-68091377, email: [support@china-core.com](mailto:support@china-core.com) or web: <http://www.china-core.com>.  
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